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Design of a Low Trans-conductance (gm) OTA

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Abstract

In recent years, there has been considerable research effort in the development of integrated OTAs with very small transconductances and improved linear range devoted for implementing analog active filters with very low cut-off frequencies. A family of CMOS operational transconductance amplifiers (OTAs) has been designed for very small g_m with transistors operating in weak inversion. A detailed comparison is to be made among different schemes in terms the transconductance, device parameters and the bias current.

Keywords: *transconductance-ota -bias current Weak inversion-source degeneration-bulk driven Common drain source degeneration*

INTRODUCTION

An operational transconductance amplifier(OTA) is a voltage controlled current source(VCCS). A group of voltage controlled circuits can use OTA as the basic active element, especially for low frequencies. The OTA gm parameter could be possibly tuned by properly choosing the device parameters of the MOSFETs such as its width(W), length(L) and also the DC bias current(Idc), supplied to the OTA circuit. The figure 1., shows the symbol and equivalent circuit of the OTA. The transconductance gm would be dependant upon the dc current Iabc. The basic forward transconductanceof the amplifier is given by the following equation,

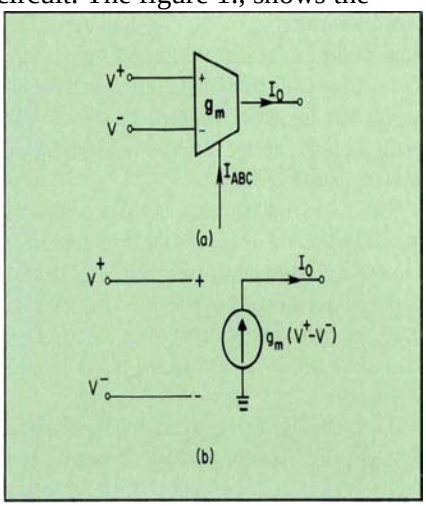


Fig. 1. a. Symbol OTA b.

Equivalent circuit(ideal OTA)

$$g_m = hI_{ABC}$$

OTA based structures are easier to implement and attractive to integrate when compared to voltage controlled voltage sources. For e.g., a second order filter would require only two OTAs and two capacitors. OTAs have extensive range of linearity and easy accessible external DC bias current which plays a very vital role in tuning the transconductance of the OTA. The basic output current of the amplifier is given by the following equation,

$$I_o = g_m(V^+ - V^-)$$

OTAs are extensively being used for the design of the filter structures in order to obtain sharp cut-off frequencies without a large passive resistor. An ideal transconductor has

an infinite bandwidth, infinie input and output impedances.

OTA TOPOLOGIES

Different topologies of the transconducatnce amplifiers have been discussed below,

1. Simple Transconductor: The nMOS configuration shown in fig. 2. is a simple

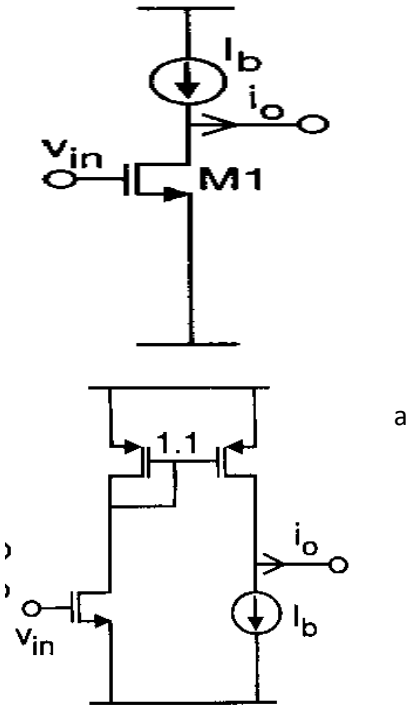


Fig. 2 a. Negative Simple Transconductor b. Positive Simple Transconductor

transconductor. Typical simplest transconductor has an nMOS driver M1 being operated in saturation region with a single input. The drawback of the configuration is that it has a very low output impedance. Several configurations are discussed further with the elimination of these drawbacks. Fig 2 a. shows a negative transconductance configuration. If a positive transconductance is desired, then, the configuration shown in fig 2 b. can be used.

2. Cascode Transconductor: The c uits shown in fig. 3. are a group o ascode transconductors. Fig. 3 a. is a simple cascode transconductor with two inputs. All the cascode transconductors will have a very high output impedance.

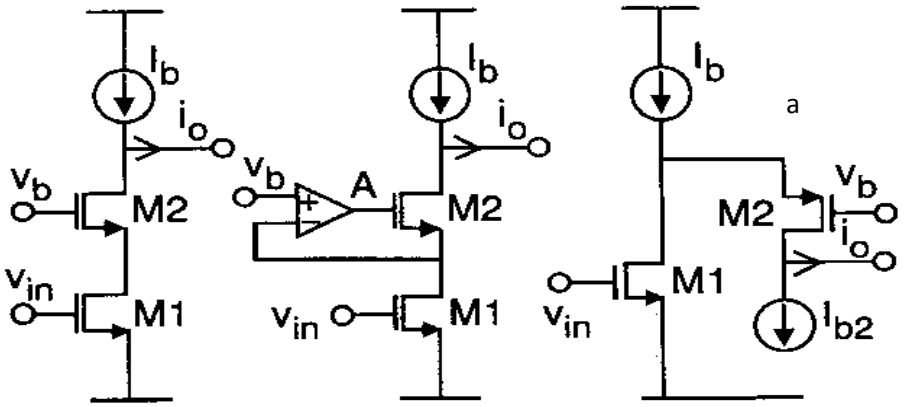


Fig. 3 a. Cascode transconductor b. Enhanced transconductor c. Folded-cascode transconductor

Better linearity is achieved in the case of a. and b. due to the ohmic region operation of the transistors. But, the transconductance is reduced when compared to the one operating in the saturation region. A simple amplifier A can further increase the output impedance of the cicuit in b. M2 transistor could be replaced by a BJT in fig. 3 b. The fig 3. c. shows a folded-cascoded transconductor. Also, a simple MOS inverter or a BJT inverter can be used in place of the amplifier. Summary of the properties of the different simple trasnconductors have been shown in the table below.

Structure/ Figure	R_{out}	Min V_{DD} *
Simple/1a	$\frac{1}{g_{ds1}}$	$\sqrt{\frac{2I_B}{k(W/L)}}+V_{Tn}+V_{sat,I_B}$
Cascode/1b	$\frac{g_{m2}}{g_{ds1}g_{ds2}}$	$\sqrt{\frac{2I_B}{k(W/L)}}+V_{Tn}+V_{sat,I_B}$
Enhanced/1c	$\frac{Ag_{m2}}{g_{ds1}g_{ds2}}$	$\sqrt{\frac{2I_B}{k(W/L)}}+V_{Tn}+V_{sat,I_B}$
Folded/1d	$\frac{g_{m2}}{g_{ds1}g_{ds2}}$	$(1+m)\sqrt{\frac{2I_B}{k(W/L)}}+V_{Tn}+V_{sat,I_B}$

The table above describes the ROUT and VDD minimum for different simple and cascoded transconductors. The ideal output transconductance of these transconductors, is infinite, but, non-ideally, it is Rout. We infer that, the output resistance increases with the decrease in the reverse transconductance gds. Also, min. VDD could be adjusted by deciding upon the device parameter ratio W/L. Cascoded and enhanced transconductors, both have the same output resistance, but due to the usage of the amplifier A, the output resistance in the enhanced transconductance is enhanced or improved ny a factor A, which is the amplifier gain. Folded cascoded and simple cascoded transconductors have the same min. VDD but due to the usage of the additional current sink at M2, the VDD is multiplied by a factor (1+m). The tabulations are helpful in choosing the right transconductor depending upon the application specifications and requirements. Also, if we want to have min. VDD, then W/L must be large. Therefore results in a large transistor size which is a trade-off.

3. Differential OTA: This section describes the OTAs with differential inputs.

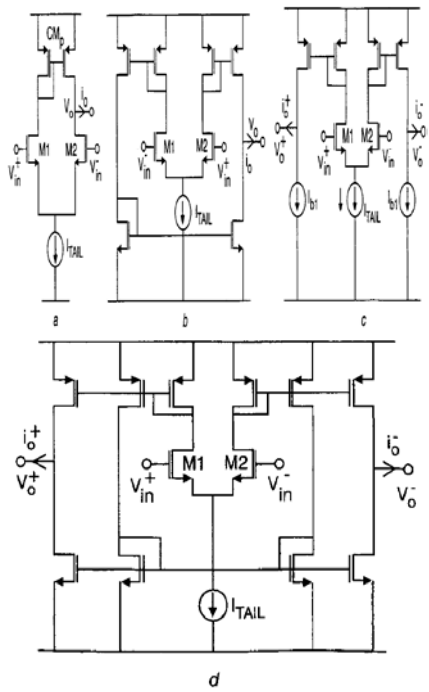


Fig. 4 a. Simple differential OTA b. Balanced OTA c. Fully differential OTA without CMF d. Fully differential OTA with CMF

The differential OTAs shown in fig 4. have the differential inputs. Very high outuput impedance can be achieved by using these OTAs as amplifiers for the cascode transconductors. Frequency compensation can also be achieved with the differential OTAs to ensure

stability. Fig. 4 a. shows a very basic and simple form of the differential OTA with the two drivers M1 and M2 and a simple current mirror load. Fig 4 b. shows the Balanced OTA which has two current mirrors and the current through whole circuit is controlled by the tail Iss i.e. the bias current. The current through the circuit is evenly distributed by the usage of the tail current source. When current increases in one of the branches, contradictarily, on the other branch, the current is pulled down to decrease. Hence, the current is balanced in the circuit. Fig. 4 c. shown is a fully differential OTA without the Common Mode Feedforward(CMF). Fig. 4 d. shown is a fully differential OTA with the Common Mode Feedforward(CMF). This is typically a symmetric architecture. Improvements have been carried out in the perview of the complexity, robustness of the circuits but not in the usage of high frequency applications. Hence, there exists a trade-off between, speed and accuracy.

LINEARISTAION TECHNIQUES

All the structures discussed in the previous sections are non-linear i.e., with a very small input range, they give 1% Total Harmonic Distortion(THD). So, to account for this, we need several techniques in order to achieve linearistaion. These are the linearistaion techniques. Following three techniques can possibly be used for linearisation:

1. Attenuation
2. Non-Linear terms cancellation
3. Source degeneration

Ideally, the output current of a differential pair is give n by the following equation:

$$i_O(v_1, v_2) = (v_1 - v_2)g_m$$

Assuming the non-linearities in practical, the general current equation is as follows:

$$i_O(v_1, v_2) = \sum_{i=1}^{\infty} a_i v_1^i + \sum_{i=1}^{\infty} b_i v_2^i + \sum_{i=1}^{\infty}\sum_{j=1}^{\infty} c_{ij} v_1^i v_2^j + I_{OS}$$

From the above equation, we can infer that the input voltage has to be made small such that the output current is given by:

$$i_O(kv_1, kv_2) = I_{OS} + \sum_{i=1}^{\infty} k^i a_i v_1^i + \sum_{i=1}^{\infty} k^i b_i v_2^i + \sum_{i=1}^{\infty}\sum_{j=1}^{\infty} k^{i+j} c_{ij} v_1^i v_2^j$$

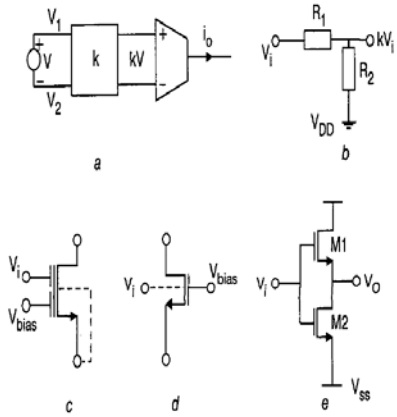


Fig 8. Attenuation technique

Thus, an attenuation of the signal by a factor k could provide the linearisation. So, an Fapproximate output current can be given as follows:

$$i_O(v_1, v_2) \cong kg_m(v_1 - v_2)$$

Fig. 8 shows several possible ways of attenuation technique. Fig 8 a. shows the concept and 8 b. shows the attenuation used for a commercial discrete OTA. Fig. 8 c. shows the floating gate technique used for the differential pair linearistaion. This results in a capacitance divider network which has Ci and Cbias. Fig 8 d. shows a bulk driven technique. Fig 8 e. shows an active attenuation technique for the drivers. All these schemes have a drawback of power consumption and increased area, since, it operates on an attenuated signal, it requires the transconductance gain to be matched. Hence, the drawbacks.

A variation of this transconductor can be obtained by keeping both top and bottom transistors in the saturation and ohmic regions respectively. So, to acheive this, the input signals are applied to the bottom trnsistors and the specific gate bias voltage is applied to all the transistors. Fig 9. shows the possible ways of non-linear terms cancellation techniques.

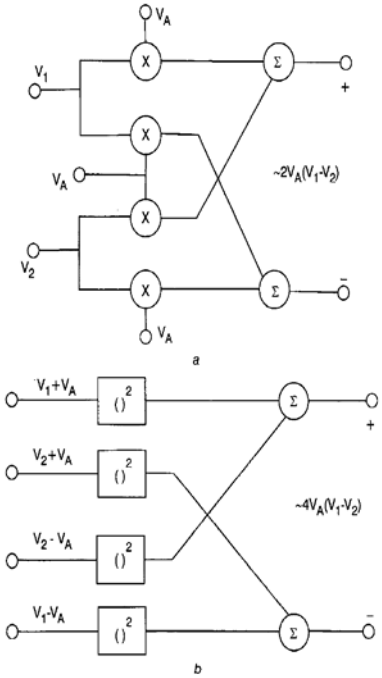


Fig. 9. Non-Linear terms cancellation technique

Linearisation techniques including source degeneration are the most widely used scheme. Fig 10. shows the possible ways of implementing the source degeneration technique. Although both the ways look alike, they present different properties and present same transconductance. Fig. 10. a. has noise contribution at the current sink, being divided into

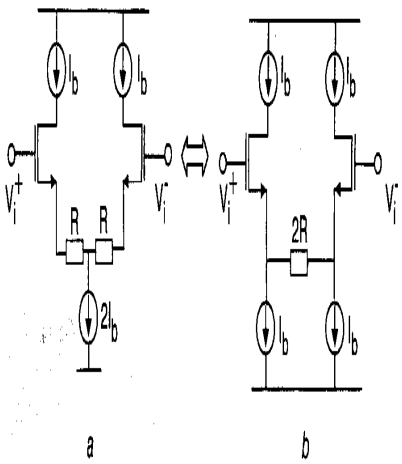


Fig. 10 Source degeneration technique

both the branches, appearing at the output as common mode noise. The voltage drop at the resistors will decrease the swing of the input signals, which is very much critical for a low voltage application. The configuration in fig. 10. b. has the noise contributions from each current sink being presented at the output branch and appears as a differential noise. The output current is given as follows:

$$i_{o,sd} = \sqrt{1-\left(\frac{v_{id}}{2(1+N)V_{DS(sat)}}\right)^2} \times \left(\frac{\sqrt{2\mu_n C_{OX} I_B \frac{W_n}{L_n}}}{1+N}\right) v_{id}$$

where, N=Gm.R, is the source degeneration factor. While, this linearisation technique reduces the small signal transconductance by a factor (1+N), the Third Harmonic Distortion is reduced by the square of the same factor.

REFERENCE OTA

The circuit hswn in the fig. 5 is a schematic of the reference operational transconductor

amplifier(OTA). The reference OTA consists of an external dc bias current source, 3 simple

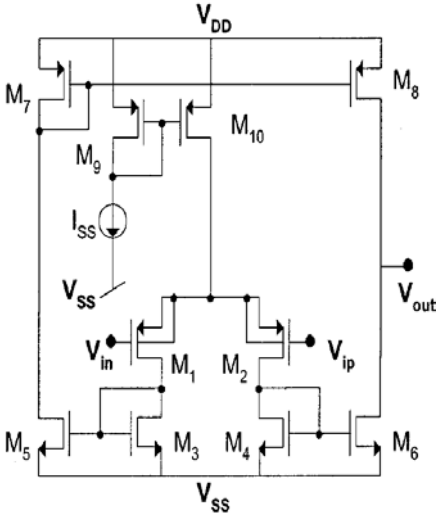


Fig. 5. Reference OTA

current mirrors and a differential amplifier stage. M1 and M2 constitute the differential pair of the circuit. M9 and M10 form the current mirror to maintain the drivers in the differential pair to operate in the required region of operation viz., strong inversion, weak inversion or moderate inversion. The overall transconductance of the circuit is the same as that of the transconductance of the drivers i.e., M1 and M2(with M3=M4=M5=M6 and M7=M8). To achieve very small transconductances, we need very low bias currents and hence, W/L ratios will be of the order of 0.001 or less. So, to match such geometrics is quite a challenge. So, we take an inversion factor *if* i.e., Id/Is. To design, we consider the different operating region considerations and obtain Id and Is value for the MOSFETs. W/L ratios are also decided using the current equations of Id and Is in different regions of operations. Desgining the MOSFETs is discussed in detail in the design section of reference OTA. The current mirrors in the reference OTA are operated in the strong inversion region for a better matching.

DEISGN

The transistors in the OTA has to be operated under 3 differnet regions:

1. Weak inversion
2. Moderate inversion
3. Strong inversion

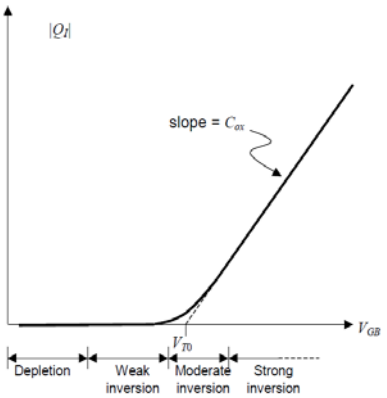


Fig 6. Regions of operation of MOSFET

The exponential relationship between the 3 regions of operation could be known by redrawing the plot in fig. 6 with a logarithmic y-axis, as shown in fig. 7.

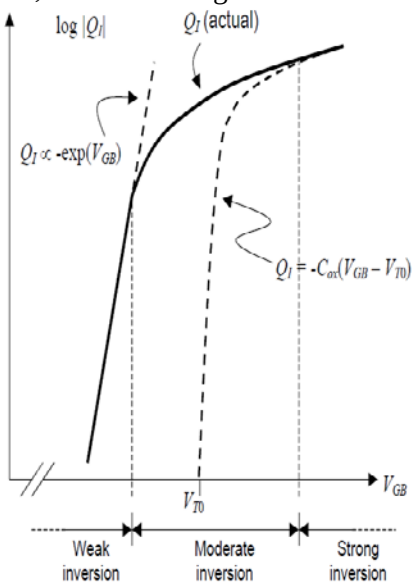


Fig. 7. Exponential relationship between 3 regions of operation of MOSFET.

All the three regions are differentitaed based upon their Vgs

and (Id,Is) values. The fig 6. shows the plot of the drai current v/s the gate voltage for a MOSFET. The differnet regions of the MOSFET are based upon following equations:

$I_D > 10I_S$	strong inversion
$10I_S > I_D > 0.1I_S$	moderate inversion
$I_D < 0.1I_S$	weak inversion

Also, the gate voltages are also decided, based upon the following consideration:

$V_{GS} > V_T + 100\text{mV}$	strong inversion
$V_T + 100\text{mV} > V_{GS} > V_T - 100\text{mV}$	moderate inversion
$V_{GS} < V_T - 100\text{mV}$	weak inversion

From the considerations above, we decide upon the gate voltage and the drain, source currents of the MOSFETs, such that the MOSFET is in the required region of operation. Later, we calculate the W/L ratios of the MOSFET using the following equations:

$$I_D = I_0 \frac{W}{L} \exp\left(\frac{\kappa V_G - V_S}{U_T}\right) \cdot \left[1 - \exp\left(\frac{-V_{DS}}{U_T}\right)\right]$$

$$I_S = \frac{2\mu C'_{ox} U_T^2}{\kappa} \frac{W}{L}$$

where, UT is the Thermal Voltage, UT = kT/q=26mv at room temp.(approx.)

k is the gate coupling co-efficient=0.7(approx.)

CALCULATIONS

To calculate Is:

up=0.0063, Cox=2.2m, UT=26mV, L=180nm.

Using Is equation given under design section,

with W=1um, Is=104.74282nA

10Is=1047.4282nA, 0.1Is=10.474282nA

Similarly, with W=400nm, Is=41.8997128nA

10Is=418.97128nA, 0.1Is=4.1897nA

RESULTS

1. WEAK INVERSION

since, Id<0.1Is and VGS<=VT-100mV. VT=0.43V

therefore, VGS=150mV.

for 0.1Is=10.474282nA and W=1um, Vds=30mV

Id=78pA(approx.)

with W=400nm,

Id=32pA(approx.)

2. MODERATE INVERSION

since, 10Is>Id>0.1Is and VT+100mV>VGS>VT-100mV

therefore, VGS=450mV. VDS=30mV

with W=1um

Id=176nA(approx.)

with W=400nm

Id=71nA(approx.)

3. STRONG INVERSION

since, VGS>VT+100mV and Id>10Is. Therefore, VGS=720mV and VDS=400mV,

W=1um

Id=369uA(approx.)

with W=400nm

Id=148uA(approx.)

CURRENT MIRRORS:

Assuming Ids, using the Id equation in saturation region, we get W values.

Therefore, for Ids=78pA, W=70nm.

Now, using the relation,

Id/Iref=W2/W1,

With, Id=2nA, Iref=78p and W1=70nm,

W2=2um(approx.)

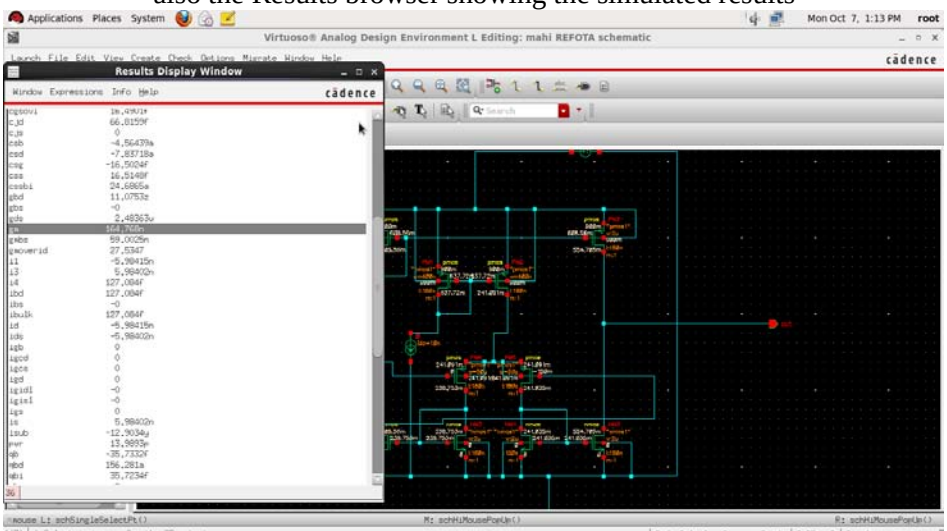
Similarly, we design the values at different regions and different current values.

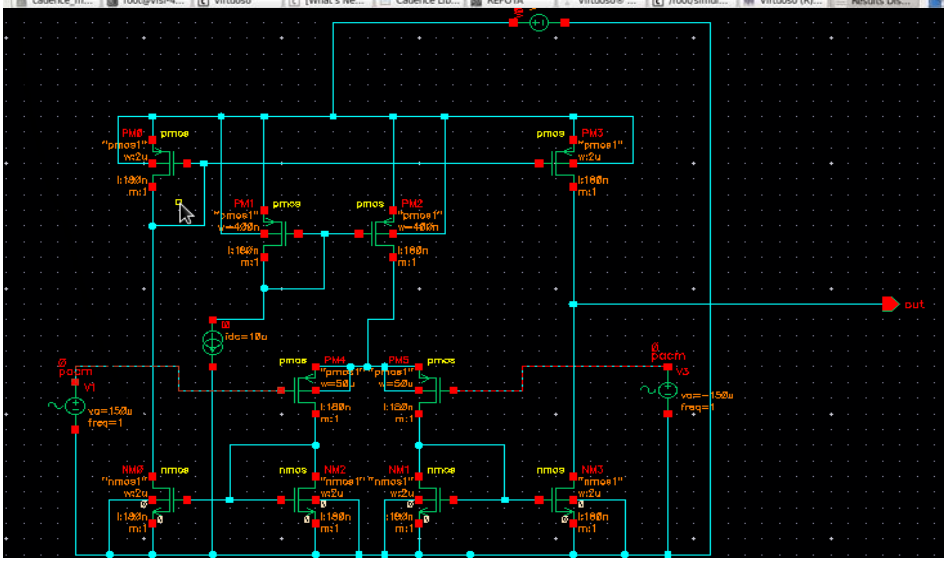
When the width is constrained in the tool, we can go for nearest value, till we have our devices at required operating regions.

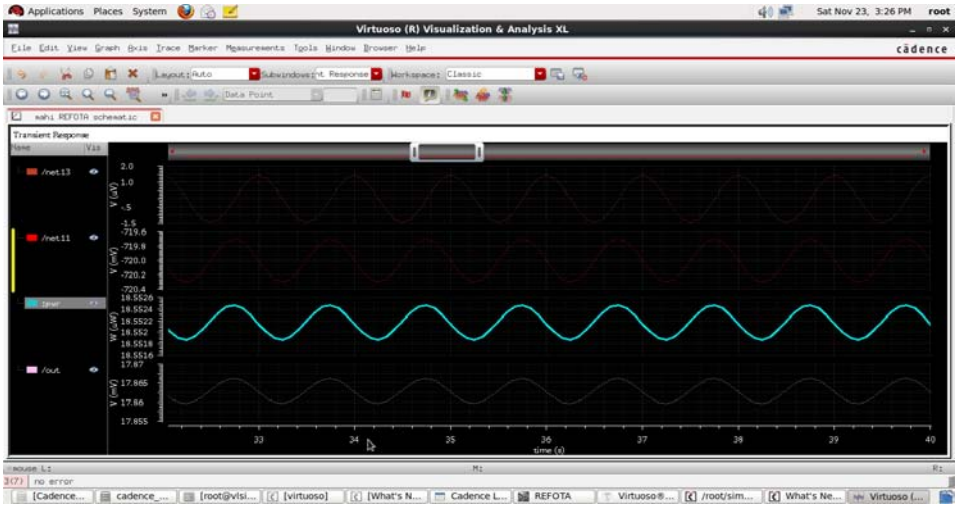
The circuit was designed and simulated using the CADENCE VIRTUOSO simulator tool and following results were tabulated.

REGION	Iss(A)	W(m)	L(m)	Gm(S)
WEAK INVERSION	2n	50u	180n	34.1206n
WEAK INVERSION	2n	400n	180n	30.763n
STRONG INVERSION	10n	50u	180n	112.531n
STRONG INVERSION	10n	400n	180n	34.0117n
MODERATE INVERSION	10u	50u	180n	89.4u
MODERATE INVERSION	10u	400n	180n	21.352u

Following screenshots are of the circuit design in CADENCE VIRTUOSO and also the Results browser showing the simulated results







CDSD-OTA

The (Current-Division Source-Degeneration)CDSD-OTA is actually a combiation of following two schemes:

1. Current division(Current Splitting)
2. Source degeneration

Current Division Scheme

The schematic shown below describes the current division technique. The scheme

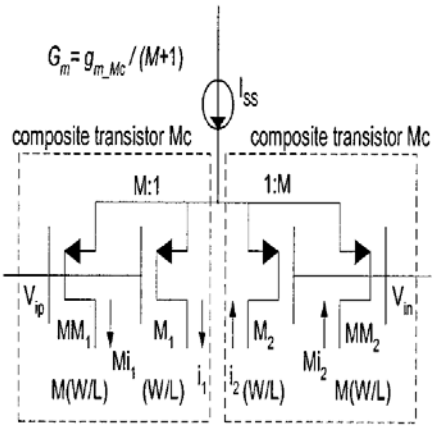


Fig 8. Current splitting using a composite transistor

starts with the Iss current flowing through a composite transistor Mc and gets divided in a ratio M:1. The currents i1 and i2 are then used after splitting. The effective Gm is given by

$$G_m = g_{m\_Mc} / (M+1)$$

Therefore, the transconductance will now be reduced by a factor (M+1) when compared to the one before current splitting.

Source Degeneration

The schematic shown below describes the source degeneration scheme. The scheme

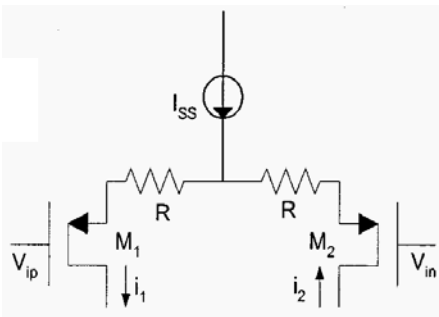


Fig 9. Source degeneration scheme

starts with the Iss current flowing through the source connected transistors. The transistors are maintained at triode region such that, both act as large resistances. The main idea behind the source degeneration is using these resistances so that the transconductance of each transistor gets reduced by the resistance. Therefore, the overall transconductance will get reduced by a factor equal to product of

resistance and the individual transconductance.
The overall transconductance of the scheme is given by

$$G_m = \frac{g_{m\_M1,2}}{1 + g_{m\_M1,2}R}$$

It is clear from the equation that, the effective Gm would be decreased by a factor of (1+gm.R). Also, source degeneration linearisation is achieved.

Hence, following the observations in above schemes presented, both the schemes were combined together to achieve the low transconductance

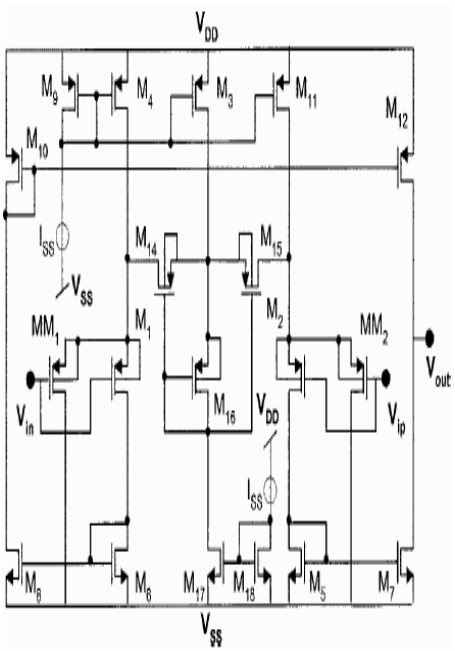


Fig 10. OTA with CDSD scheme

The above figure clearly illustrates that the current division is applied at the MM1, MM2 transistors respectively. M14 and M15 act as the source degeneration transistors. Transistors M17, M18, M3 and M16 transistors are to maintain the source degenerators in the triode region by controlling the Vsg of M14 and M15. All the driver transistors are designed similar to the reference OTA to operate in weak inversion region. Source degenerators are designed as per the resistance value. Transistors M5 through M7,M10 and M12 must be of equal sizes, since they are just copy circuits for outputs. The overall transconductance of the circuit is given by

$$G_m = \left(\frac{g_{m\_M1,2}}{1 + \frac{(M+1)g_{m\_M1,2}}{g_{0\_M14}}} \right)$$

where, M is given by,

$$M = \frac{g_{m\_MM1}}{g_{m\_M1}}$$

Hence, from the effective Gm equation, it is very much clear that, the overall transconductance of the driver is reduced by a factor of [1+(M+1)(gm_M1/g0_M14)]. The factor (1+M) is due to the transistors MM1 and MM2 which will divert the major portion of the bias current through the rails. G0_M14 is the output transconductance of the transistor M14 which is clearly just the reciprocal of R. It can be controlled by the Bias current Iss. The G0_M14 is given by

$$g_{0\_M14} = n\mu C_{0x} \frac{W_{M14}}{L_{M14}} (V_{SG\_M14} - |V_{TP}|)$$

Hence, the current division scheme clearly helps in enhancing the current levels while maintaining the lengths of transistors as small.

CALCULATION

To find the effective Gm

the transconductance value of the source degenerator is obtained from the simulation window
gm_M14=1.1794nA/V.
Therefore, the resistance R=848M ohm(approx.)
Now, gm1 is calculated from the source degenration formula for the

transconductance.
gm1=510.118pA/v.
gm_MM1 is found from the result browsers and M is calculated.

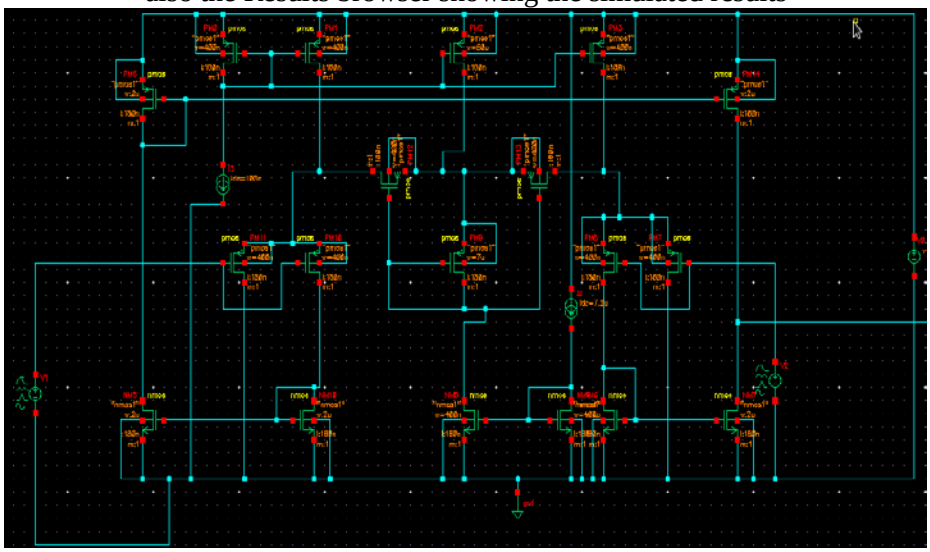
Using the effective Gm formula discussed under the CDSD OTA section, the Gm value is calculated.
M=2.857, g0=929.7nA/V and gm_M1=356pA/V
Gm=356pA/V(approx.)

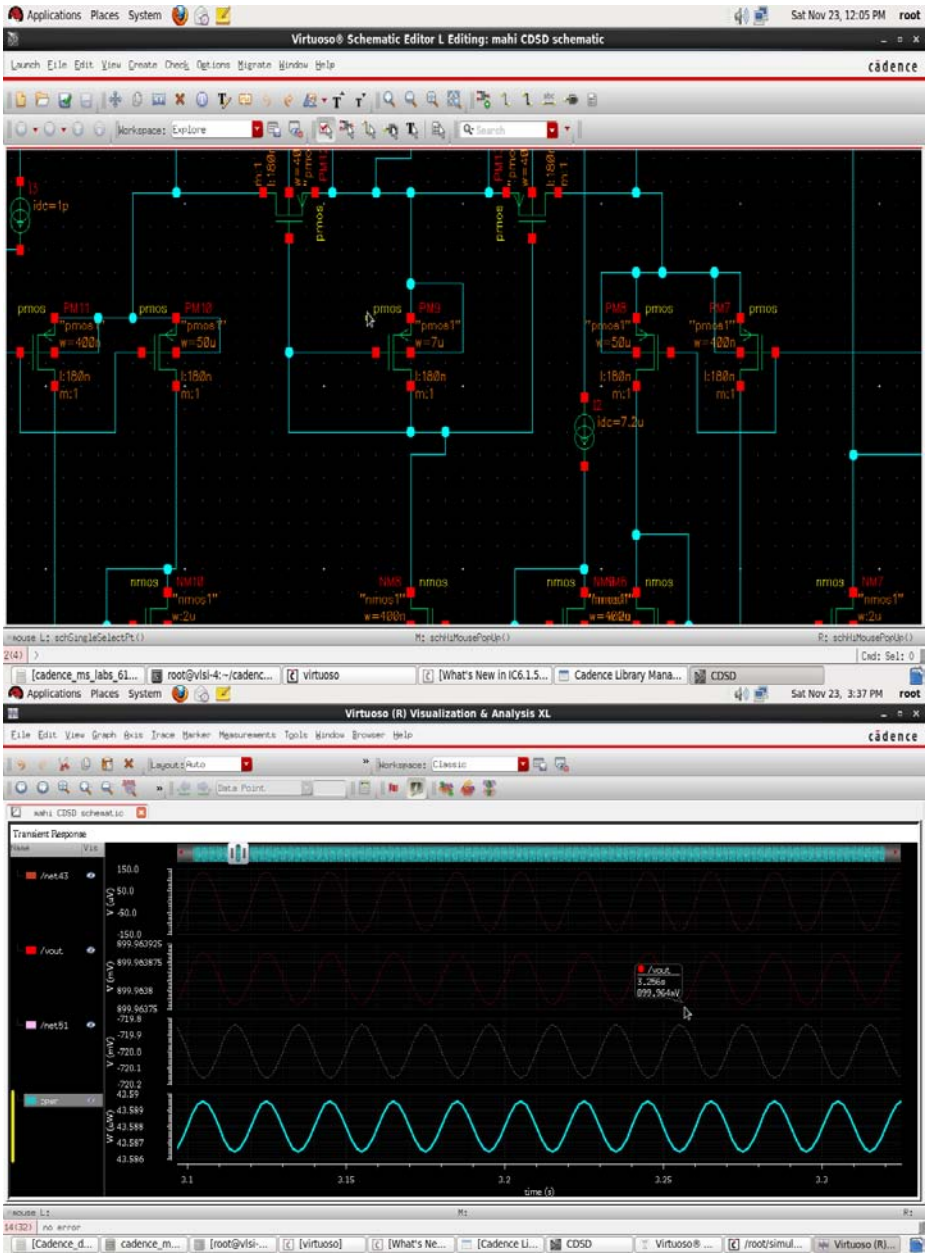
RESULTS

The circuit was designed and simulated using the CADENCE VIRTUOSO simulator tool and following results were tabulated.

Iss(A)	W(m)	L(m)	Gm(S)
1n	50u	180n	2.291n
	400n	180n	192.73p
10n	50u	180n	2.474n
	400n	180n	2.727n
100n	50u	180n	964.43n
	400n	180n	130.33n

Following screenshots are of the circuit design in CADENCE VIRTUOSO and also the Results browser showing the simulated results





BULK-DRIVEN CDSD-OTA

The bulk-driven technique incorporates the basic CDSD scheme with the drivers being driven at the bulk rather than the gate. This increases the linearistaion of the circuit as well as further reduces the transconductance. The gmb of the drivers in the scheme is almost 0.2 to 0.4 times the Gm. It is very much process dependent.

BASIC PRINCIPLE

Consider a basic differential pair which has bulk driven transistors as its drivers.

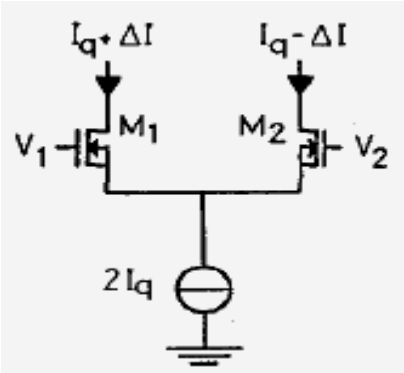


Fig 11. Bulk driven simple differential pair

Now, from fig 11, we see that both M1 and M2 are driven at bulk instead of its gate. Also, the bulk and source are connected to each other. Therefore, the drain current of the transistors in weak inversion and saturation is given by

$$I_D = I_{D0} e^{\frac{V_{GS}+(n-1)V_{BS}}{nU_T}}$$

From the above equation we can infer that the drain current is exponentially dependant on the voltage Vbs. Clearly, by controlling the bulk source voltage(Vbs), we can control the drain current through the MOSFET. When we use a differential pair with bulk driven MOSFETs as shown in fig 11., the differential output current will be a hyperbolic tangent function of its differential input voltage. The equation for this relationship is given by

$$\Delta I = I_q \tanh\left[\frac{V_{in}}{2nU_T} + \frac{1}{2}\ln\left(\frac{I_{D01}}{I_{D02}}\right)\right]$$

This function will be scaled by approximately 1.5 as a factor when compared to that of BJTs.

To linearise the circuit further, we need an offset to be introduced. This offset can be introduced by properly adjusting (Id01/Id02). In terms of the device parameters, we can adjust the ratio of (W1/L1)/(W2/L2).

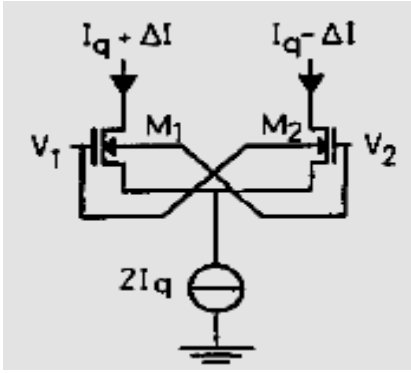


Fig 12. Extended Principle

The bulks of both M1 and M2 in fig. 11 can also be used as the active ends. To achieve this, both the ends will be connected as shown in the fig. 12. This kind of a configuration will result in an opposite variations in the bulk and gate with respect to source. The overall transconductance of the configuration is the difference between the transconductances of the gate and the bulk. The equivalent gmeq can be given by

$$g_{meq} = g_{mg} - g_{mb} = g_{mg}(2-n)$$

The factor, 1/(2-n) will be the one which extends the linear range of the circuit. With such a configuration shown in fig. 12, there is a chance of having a forward biased bulk source junctions, which is highly undesired. Therefore to avoid such forward biases, we add two voltage sources at the bulk regions as shown in fig. 13.

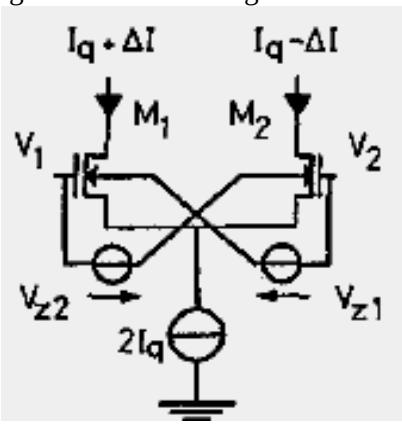


Fig 13. Extended differential pair

Due to the addition of the voltage sources at the bulk source junctions, there is a possibility of mismatches

in the threshold voltages of the devices. Therefore, the drain current(differential output) equation, now includes the threshold mismatches also. The equation is given by

$$\Delta I = I_q \tanh\left(\frac{2-n}{2n}\frac{V_{in}}{U_T} + \frac{1}{2}\frac{\Delta V_{T0}}{nU_T} + \frac{n-1}{2n}\frac{\Delta V_z}{U_T}\right)$$

where, ΔV_{T0} is the threshold voltage mismatches.

ΔV_z =Vz1-Vz2, is the mismatch between the voltages Vz1 and Vz2.

The input referred offset voltage is given by

$$V_{os} = \frac{1}{2-n}\Delta V_{T0} + \frac{n-1}{2-n}\Delta V_z$$

The noise performance of the extended differential pair will now be degraded by the factor 1/(2-n) as the effective transconductance reduction due to the contribution of ΔV_{T0}. The additional noise contribution can be achieved by using the additional transistors as shown in the fig. 14.

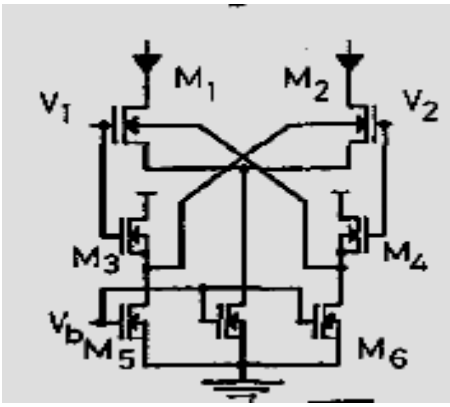


Fig 14. Extended diffrential pair with additional MOSFETs

The transistors added in the configuration shown in fig. 14 act as source followers and apply the voltages at the bulks of the drivers.

The thermal noise factor γ is used to evaluate the global noise degaradation. γ is referred as the product of the input referred-thermal noise resistance and the transconductance. The equation is given by

$$\gamma = \frac{n}{2-n_1}\left[1 + \left(\frac{n_1-1}{n_1+1}\right)^2 \frac{2I_q}{I_{sf}}\left(1 + \frac{8}{3}\frac{n_5 U_T}{V_b - V_{T05}}\right)\right]$$

where, Isf is the bias current of the source followers.

2Iq is the tail current of the diffrential pair.

SCHEMATIC

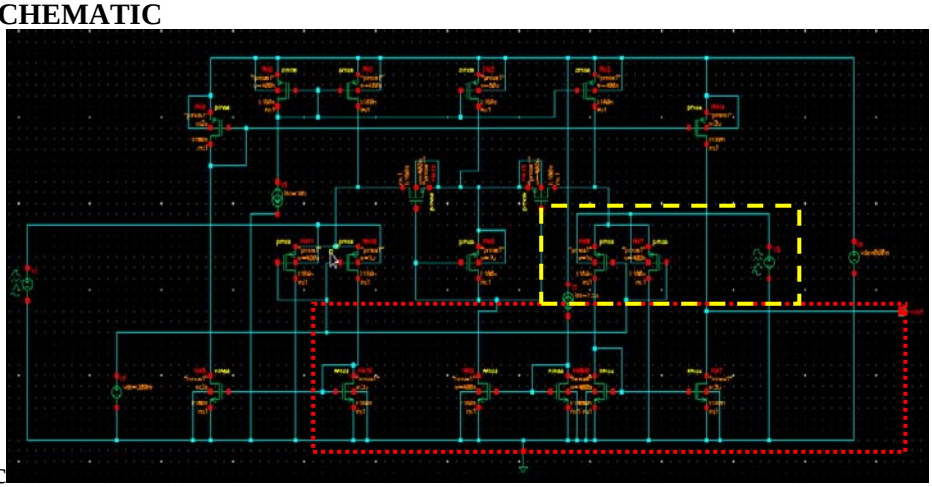


Fig 15. Bulk Driven CDSD-OTA

The above shown fig 15. is a schematic of the bulk driven CDSD OTA. The highlighted part in the red dashed box is the current division part. The portion highlighted by yellow dashed box is the source degeneration part.

In this type of a configuration as mentioned earlier, the inputs to the OTA are driven at the Bulks rather than its gates. The gates are maintained at a voltage Vg, which ensures that gate is not at zero potential and maintains the transistors at weak inversion mode. Application of the input voltages at the bulks of the drivers will give rise to the bulk source voltages. Due to the variation in the bulk source voltages, the fermi levels of the transistor will start to vary and lead to the mismatches in the threshold voltages. The mismatched threshold voltages can contribute to the degradation of the noise performance and also reduces the effective transconducatnce. Since, the circuit is already employed with the current division technique, it will have the transconductance reduction as mentioned earlier in CDSD-OTA. To reduce the transconductance again by a factor inversely proportional to the resistance of the source degenerators, the source degeneration scheme is also included. The current division scheme ensures to allow a small bias current with considerably small transistor. With the combination of all the three schemes, the effective transonductance is reduced further when compared to the reference OTA and the CDSD OTA alone.

MATHEMATICAL ANALYSIS

For all the relations made under this section, the channel length modulation is considered to be negligible. The behavior of the threshold voltage for the bulk driven devices is given by

$$|V_{TH}| = |V_{TH0}| + |\gamma|\left[\sqrt{2|\phi_F| + V_{BS}} - \sqrt{2|\phi_F|}\right]$$

where, γ_0 is the body effect parameter-approx. 0.7

φ_{FB} is the bulk-fermi potential-approx. 0.35V

VTH0 is the threshold voltage when the Vbs is zero.

When the transistors are bulk driven, the dependance of the threshold voltage on the Vbs voltage is considered, which is known as the body effect. Indeed, the drain current Id also changes with the change in Vbs causing a transconductance function in the device between the bulk and drain current.

The transconductance of a bulk driven transistor is given by

$$g_{mb} = \frac{\partial I_D}{\partial V_{SB}} = \frac{|\gamma| g_m}{2\sqrt{2|\phi_F| + V_{BS}}} = \frac{|\gamma|}{2\sqrt{2|\phi_F| + V_{BS}}}\sqrt{2\beta I_D}$$

With a properly matched values of the bulk-fermi potential and effective body effect parameters, the gmb can be 20% to 50% of the gm.

The equation for the effectiive transconductance due to the bulk driven CDSD OTA is given by

$$G_m = \left(\frac{\gamma_0}{2\sqrt{2\varphi_{FB} + |V_{BS}|}}\right) g_{m\_M1}$$

where, gm_M1 is the transcoductance of the driver

From the equation above, it is clear that this scheme is very much dependant on the process parameters. Hence, the process designers have a greater advantage than the circuit designers. All the process parameters have to be considered carefully and we see that they are well matched. Now, due to

the addition of source degeration resistors, the transconductance of gm_M1 includes the reduction factor of the source degeneration scheme. Therefore, while computing the results, the transconductance of M1 is calculated by the process mentioned in the CDSD scheme and then effective gm will be calculated using the equation above.

CALCULATION

To find the effective transconductance

gm_M14, the source degeneration transistor is obtained directly from the result browser.

gm_M1, the transconductance of the driver transistor is obtained from the result browser.

Gm_M1, the transconductance of the driver is calculated using the source degenration formula.

Total effective Gm is calculated from the formula discussed under the Mathematical analysis section.

with gm_M14=295.52pA/V, gm_M1=2.601pA/V, Gm_M1=2.5786pA/V

values of the body effect parameter anf fermi level are taken as 0.7 and 0.35 respectively.

VBS=500mV

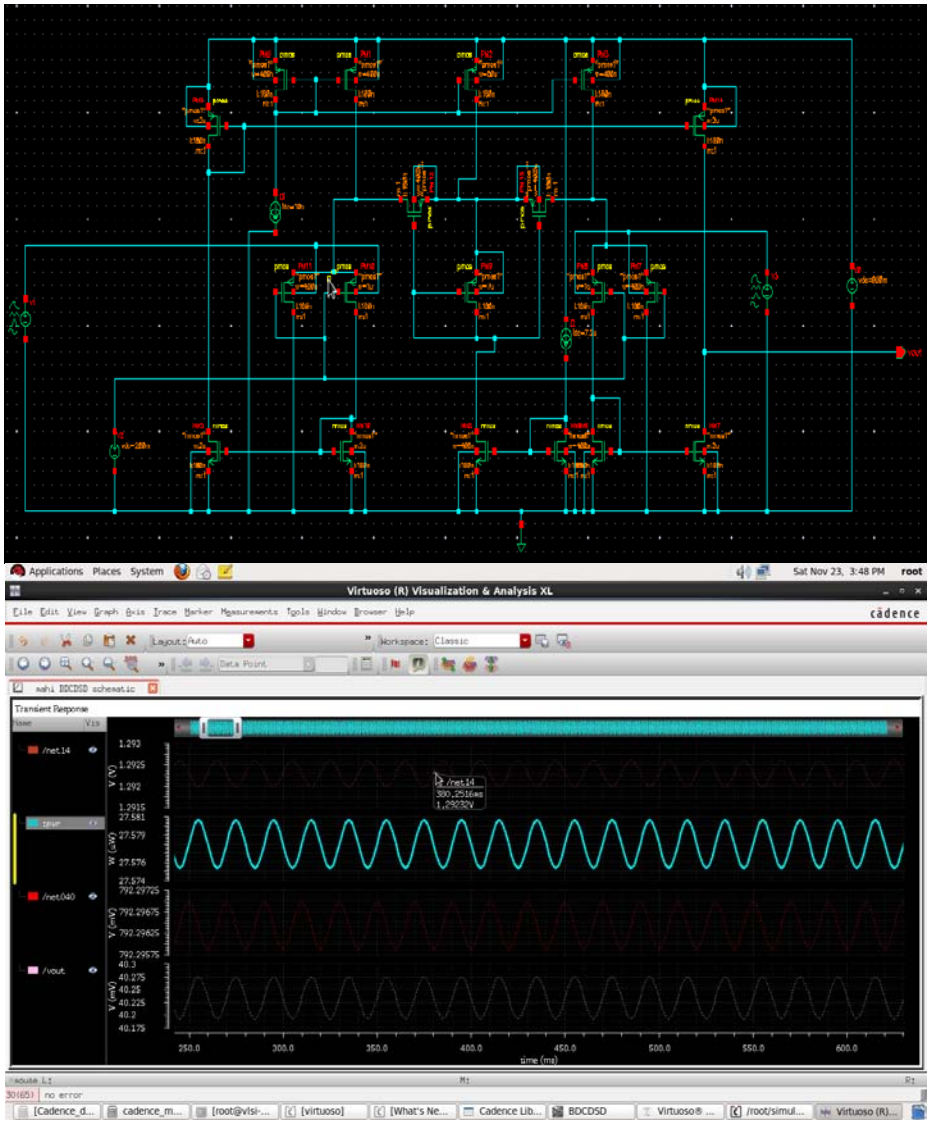
Therefore, Gm=1.1pA/V(approx.)

RESULTS

The circuit was designed and simulated using the CADENCE VIRTUOSO simulator tool and following results were tabulated.

Iss(A)	W(m)	L(m)	Gm(S)
1n	1u	180n	12.326p
	50u	180n	628.41p
	400n	180n	59.73p
10n	1u	180n	490.067p
	50u	180n	18.746n
	400n	180n	1.767n
100n	1u	180n	76.426n
	50u	180n	786.097n
	400n	180n	109.8871n
1p	1u	180n	14.225f
	50u	180n	537.48f
	400n	180n	81.9f

Following screenshots are of the circuit design in CADENCE VIRTUOSO and also the Results browser showing the simulated results



MERITS

1. Gmb is directly 20% to 50% of the Gm.
2. Extended linear range than BJTs.
3. Noise performance reduction by a factor of 1/(n-2)
4. Due to the dependancy on process parameters, process people have a greater advantage.
5. Due to the combination of both current splitting and source degeneration, the transconducatnce is reduced by an inversed factor of resistance with small currents and having considerably thin transistors.

DEMERITS

1. Very much dependant on process parameters, due to which, any small changes in the process parameters can cause a large variations in transconductance. To achieve such a stable device design is very difficult.
2. Due to the usage of source degeneration resistors, at very small currents, chances of noise contribution is high.

3. For the common mode rejection, need of common mode feedback or feedforward exists.

POWER SUMMARY

The following table summarises the power dissipations in the three OTAs viz., reference OTA, CDSD OTA and BDCDSD OTA.

SCHEME	Iss(A)	W(m)	L(m)	P(W)
REFERENCE OTA	10u	400n	180n	14.51u
	10n	400n	180n	25.25n
	1n	400n	180n	2.88n
CDSD OTA	10u	400n	180n	26.45u
	10n	400n	180n	4.104u
	1n	400n	180n	3.936u
BDCDSD OTA	10u	400n	180n	35.7u
	10n	400n	180n	4.106u
	1n	400n	180n	3.936u

TRANSCONDUCTANCES SUMMARY

The following table summarises the transconductances in the three OTAs viz., reference OTA, CDSD OTA and BDCDSD OTA.

SCHEME	Iss(A)	W(m)	L(m)	P(W)
REFERENCE OTA	2n	400n	180n	30.763n
		50u	180n	34.12n
CDSD OTA	1n	400n	180n	192.73p
		50u	180n	2.291n
BDCDSD OTA	10n	400n	180n	18.746n
		50u	180n	1.767n

APPLICATIONS

Low gm OTAs are being extensively used in the following applications:

1. Active-C filter design(of 1st and 2nd orders): The filter design mainly aims at acheiveing very sharp cut-off frequencies. To achieve such sharp cut-off frequencies, to match the low-frequency applications, it is required to use a large valued resistor while capacitance remiains constant. Therefore, this requires a large poly area to design such resistors of large value and hence, many parasitics come into picture. So, in place of a large reistance, we can use a Low-gm OTA to achieve sharp cut-off frequencies.

2. As a voltage controlled resistor: In some applications, where the resistance which is connected to the virtual ground of the OPAMP can be replaced by the OTA being connected to one end i.e., one terminal is connected to the positive terminal of the OTA and the negative terminal is connected to the real ground of the OPAMP. Hence, the resistor can now be controlled by varying the Iabc, the bias current.

3. Gilbert Cell design: Analogue multipliers are vital components in many critical communication applications like multiplications in signal processors, adaptive schemes, programable neural networks and automatic control systems. All these systmes are mostly designed using the Gilbert Cells. These Gilbert cells are designed by an array of the Low-gm OTAs. Also, one more advantage is that, in some conditions, Gilbert cell faces a dependency on the temperature, so by adding an additional OTA, these effects can be compensated.

4. Others: Control structures for tuning in OTA-C filters, generating an arbitrary piecewise linear function using non-linear functions, etc,.

HARDWARE AND SOFTWARE REQUIREMENTS

- CADENCE VIRTUOSO SIMULATOR

CONCLUSION

OTA was designed to operate in weak inversion region for 3 different schemes viz., Reference OTA, CDSD OTA and the BDCDSD OTA. All the transconductances were tabulated for the three schemes at different bias currents. Power dissipations were tabulated. We see that CDSD OTA will provide a lower transconductance than the reference OTA with an advantage of having small currents for considerably thin transistors. BDCDSD OTA will provide the lowest transconductance among the three schemes with almost the same power consumption as in a CDSD type.

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